

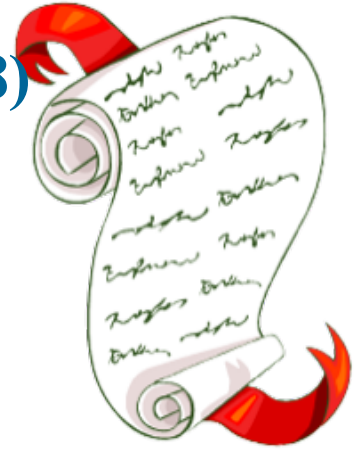




# Today's Agenda

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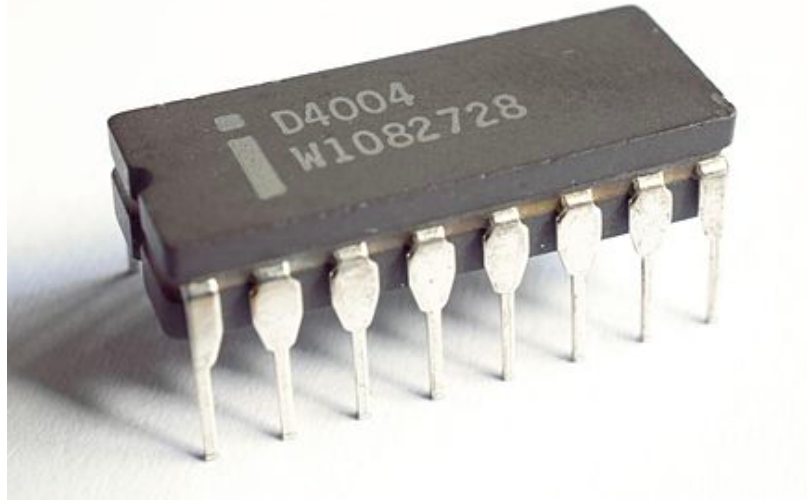
- Intel 4004 (1971)
  - Intel 8008
  - Intel 8080
  - **Intel 8086 (x86)**
  - Intel 80286
  - Intel 80386
  - Intel 80486
  - Intel 80586 (Pentium P5)
  - Intel 80686 (Pentium P6)
  - **Intel Core (2006)**
1. Intel Nehalem (2008)
  2. Intel Sandy Bridge
  3. Intel Ivy Bridge
  4. Intel Haswell
  5. Intel Broadwell
  6. Intel Sky Lake
  7. Intel Kaby Lake
  8. Intel Coffee Lake
  9. Intel Coffee Lake Refresh
  10. Intel Comet Lake (2019)





# Intel-4004: 1971

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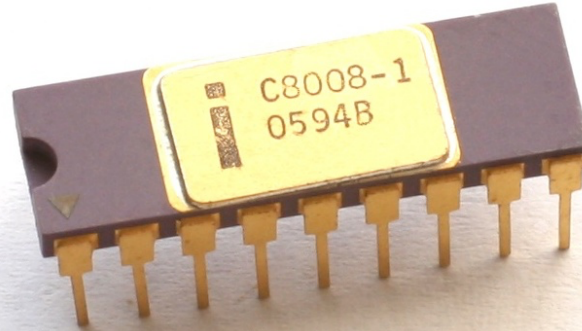
## Characteristics:

- 4-bit data bus (register/word size)
- 12-bit address bus that could address 4 KiB of memory
- 2300 transistors
- 400 – 800 KHz
- 16-pin DIP package
- One instruction took eight clock cycles to complete (Fetch, Decode Execute)
- Used in Busicom Calculator (BCD oriented)



# Intel-8008: 1972

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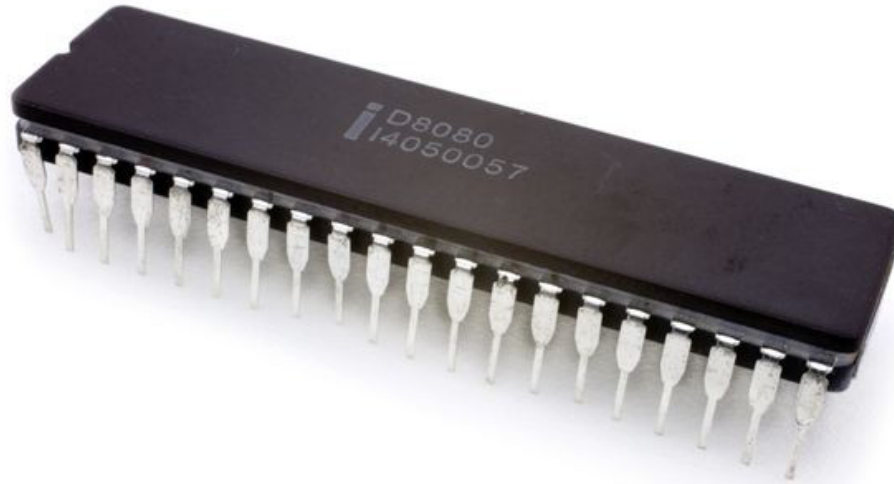
## Characteristics:

- 8-bit data bus (register/word size)
- 14-bit address bus that could address 16 KiB of memory
- 3500 transistors
- 500 – 800 KHz
- 18-pin DIP package
- Introduced the concept of interrupts



# Intel-8080: 1974

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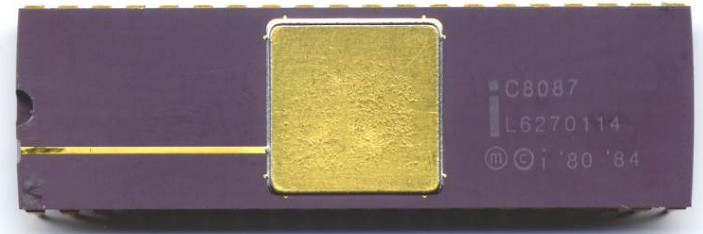
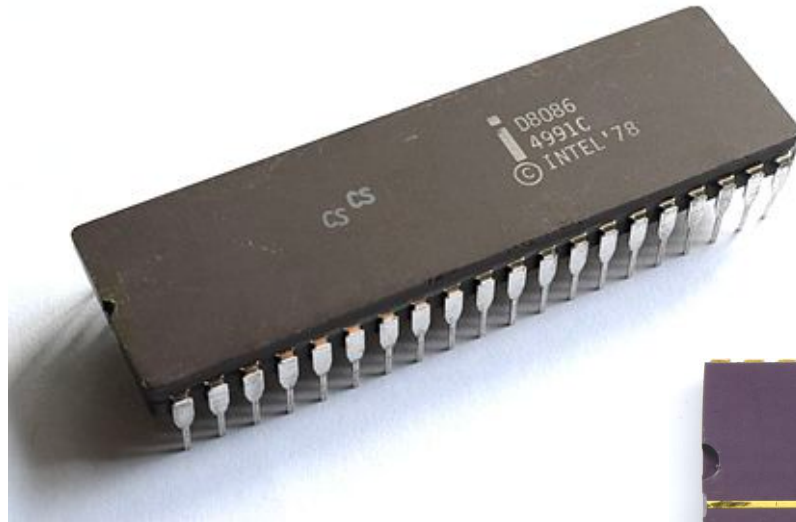


## Characteristics:

- 8-bit data bus (register size)
- 16-bit address bus that could address 64 KiB of memory
- 4500 transistors
- 2 MHz
- 40-pin DIP package



# Intel-8086: 1978



## Characteristics:

- 16-bit data bus (register size)
- 20-bit address bus that could address 1 MiB of memory
- Introduced Segmented memory model (for portability of 8080 programs)
- 29K transistors
- 5-10 MHz
- 40-pin DIP package
- Separate 8087 Floating Point Unit (Math co-processor)
- Used in low cost microcontroller now



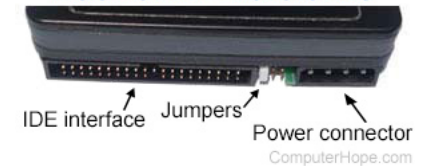
# Intel-80286: 1982



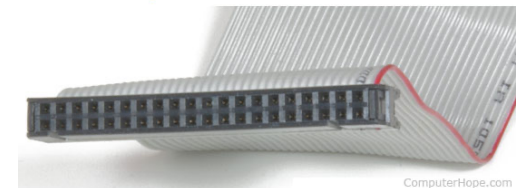
## Characteristics:

- 16-bit data bus (register size)
- 24-bit address bus that could address 16 MiB of memory
- 134 K transistors
- 20 MHz
- Separate 80287 Floating Point Unit (Math co-processor)
- Introduced the concept of Protected Memory
- Introduced IDE bus architecture
- Introduced DMA controller

## Back of IDE hard drive



40-pin IDE IDC connector and cable





# Intel-80386: 1985



## Characteristics:

- 32-bit data bus (register size)
- 32-bit address bus that could address 4 GiB of memory
- 275 K transistors
- 16-33 MHz
- Separate 80387 Floating Point Unit (Math co-processor)
- Introduced the concept of memory paging and virtual memory





# Intel-80486: 1989

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## Characteristics:

- 32-bit data bus (register size)
- 32-bit address bus that could address 4 GiB of memory
- 1.2 M transistors
- 25-100 MHz
- Built in 8 KiB cache
- Integrated FPU (Math co-processor)
- Introduced the concept of instruction pipelining
- 80486 showed 50% improved performance over 80386 processor



# Intel-80586/Intel-P5: 1993

Intel-P5 microarchitecture was introduced in 1993, which was a direct extension of the 80486 architecture and frequently referred to as i586. Pentium-I and Pentium-II were the Intel models/brands based on P5 architecture



## Characteristics:

- 64-bit data bus (register size)
- 64-bit address bus that could address 16 Exbi Byte of memory
- 3.2 M transistors
- 60-300 MHz
- 8 KiB on-chip data and instruction caches (2-way associative)
- Super-scalar design with two parallel 5-stages pipelines, so can execute two instructions per cycle
- Later versions introduced **MMX** instructions, that support SIMD operations



# Intel-80686/Intel-P6: 1997

Intel-P6 microarchitecture was introduced in 1997, which was a direct extension of the 80586 architecture and frequently referred to as i686

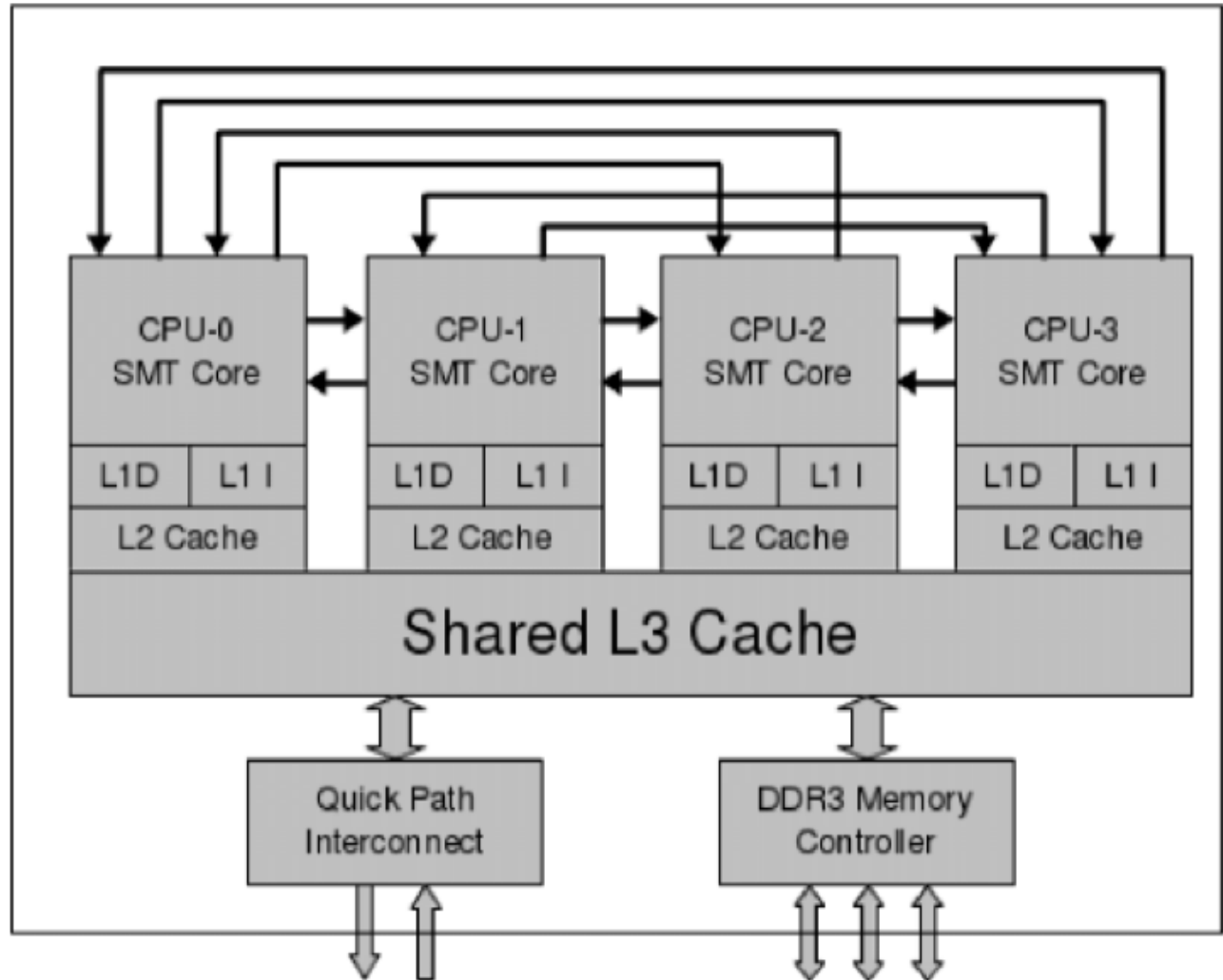


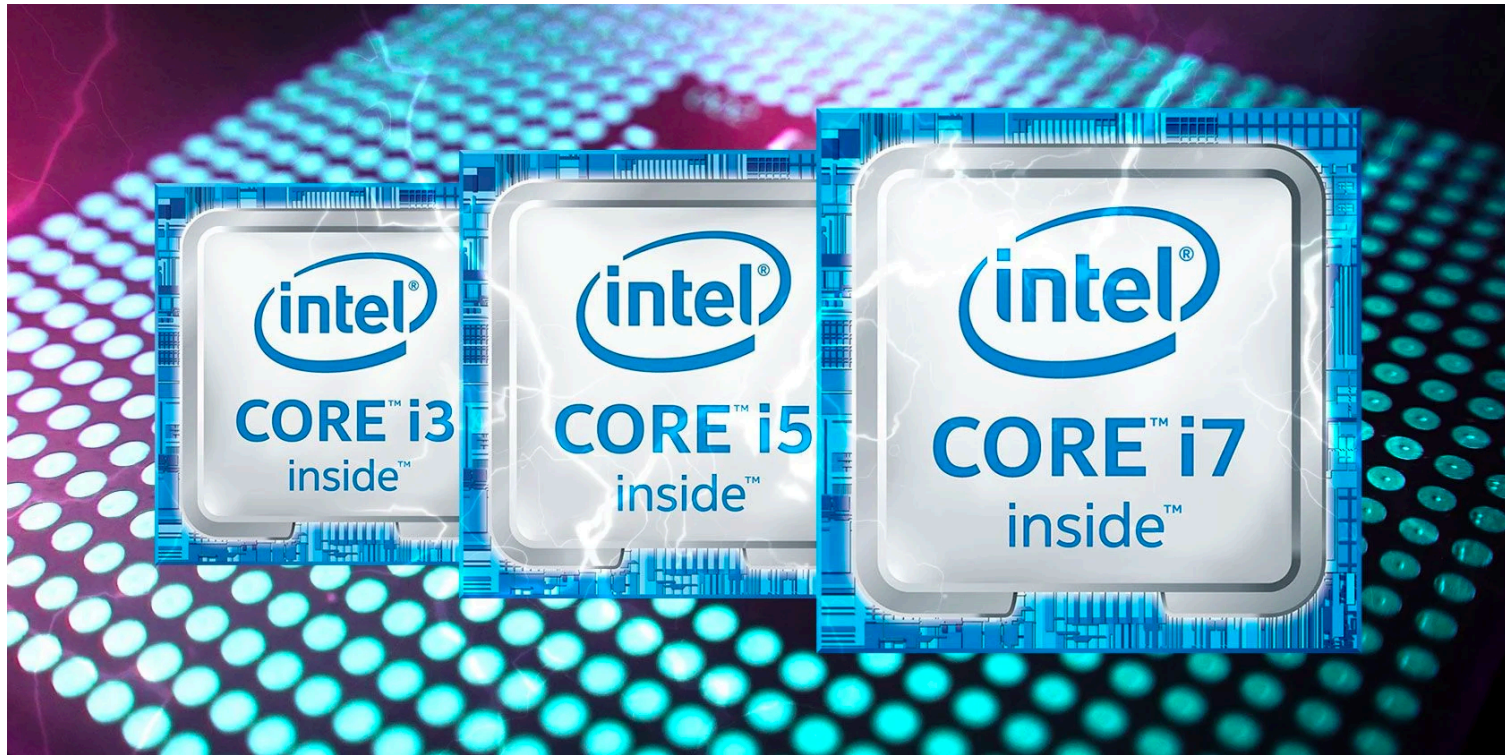
## Characteristics:

- 64 bit data/address bus and 3.8+ GHz
- 16-32 KiB on-chip data and instruction caches
- Super-scalar design with three parallel 12-stages pipeline, so can execute 3 instructions in each clock cycle
- Supports out of order execution, register renaming, improved branch prediction, and speculative instruction execution
- Pentium-III was an Intel brand/brand based on P6 architecture, which introduced a new SIMD technology called Streaming SIMD Extension (SSE)
- Pentium-IV was an intel brand/model based on p6 architecture, having a clock support of upto 3.8+ GHZ and support of hyper-threading technology



# Intel Core: 2006

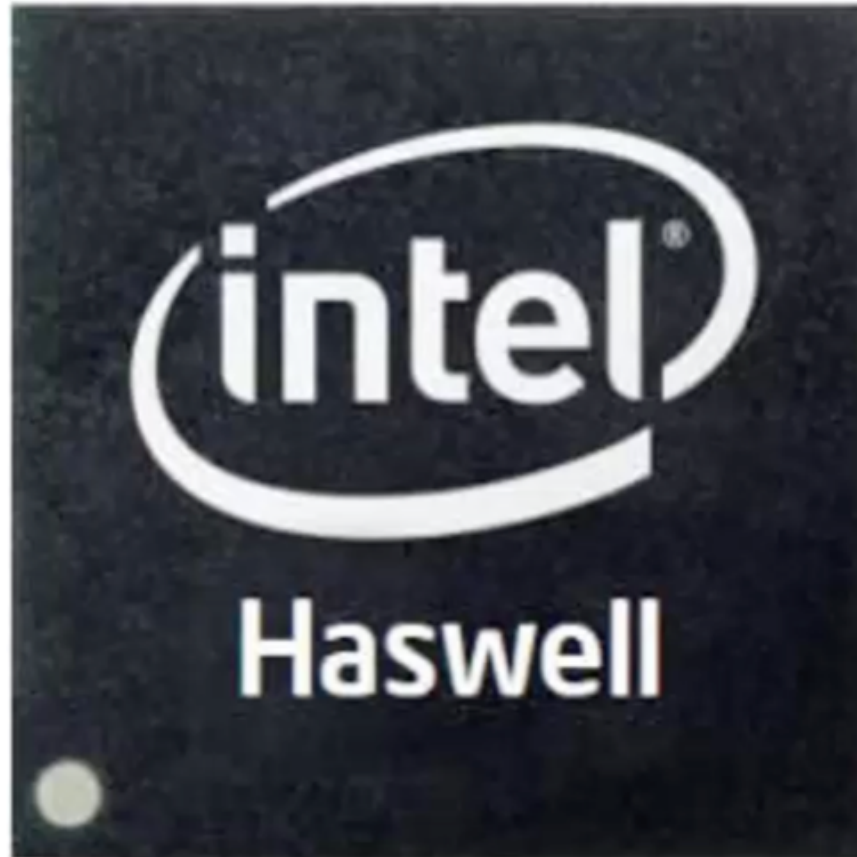




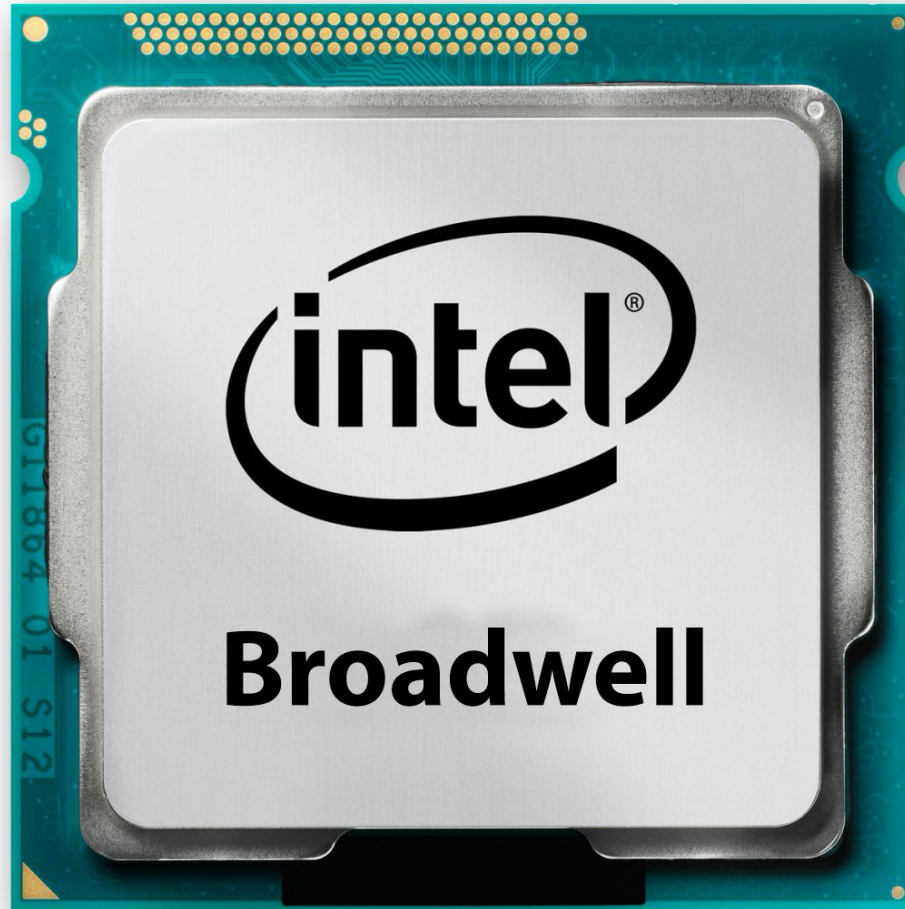
- **Corei3:** slow clock speed w/o turbo-boost, normally having 2 cores - 4 threads with HT enabled
- **Corei5:** comes with turbo-boost, normally having 4 cores - 4 threads with HT disabled
- **Corei7:** comes with more cores, more clock speed and more cache. Normally have 8 cores - 16 threads with HT enabled















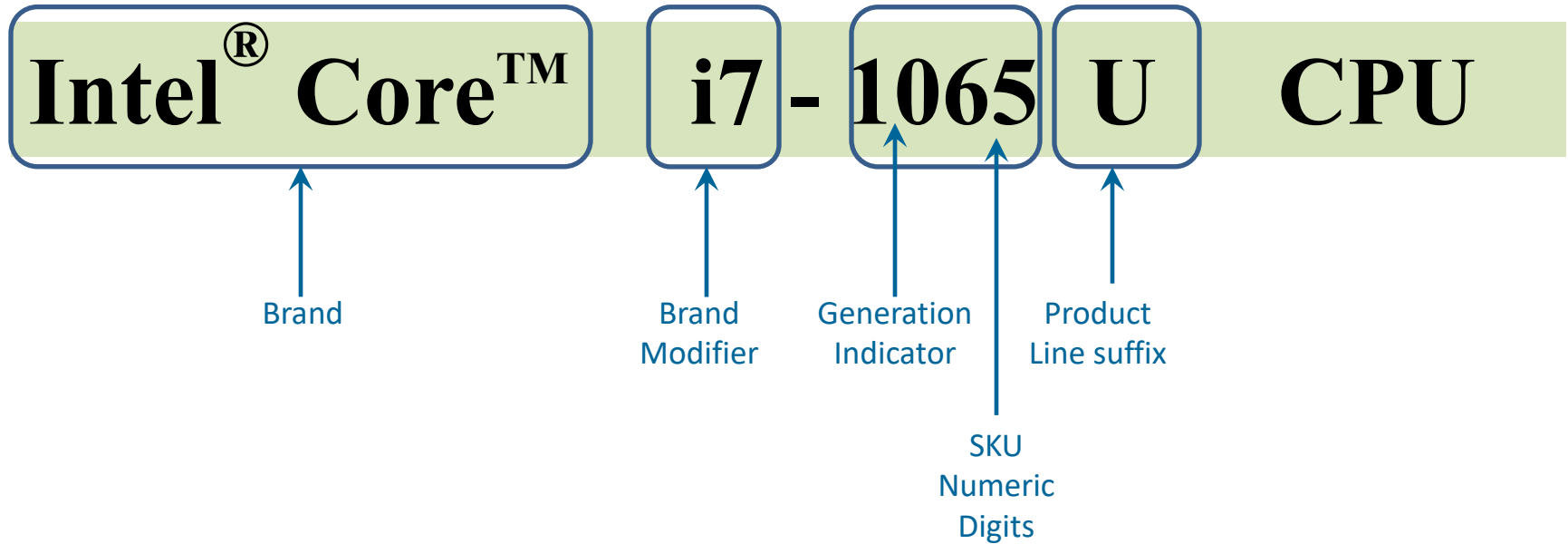








# Latest Intel Processors Naming Convention





# Things To Do

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**Coming to office hours does NOT mean you are academically week!**